Jiwon Lee

Ph.D. in Computer Architecture | Suwon, South Korea jiwon24.lee@gmail.com | jiwon.lee@yonsei.ac.kr Website | LinkedIn | Google Scholar | ORCID

I completed my Ph.D. at Yonsei University under the supervision of Professor Won Woo Ro, with a dissertation titled 'High-Performance Address Translation Mechanisms for Graphics Processing Units.' My research interests span a broad range of topics within computer architecture and systems, including (but not limited to) designing efficient CPU and GPU microarchitectures, virtual memory frameworks, scalable memory management methods. To broaden my experience, I am currently working as an engineer at Samsung Electronics.

PROFESSIONAL EXPERIENCE

Staff Engineer Samsung Electronic Memory Division, Korea Aug. 2024 - Present

Graduate Research Assistant Yonsei University, Korea Mar. 2014 - Aug. 2018

Embedded Systems and Computer Architecture Lab (eSCaL)

Advisor: Won Woo Ro

EDUCATION

Doctor of Philosophy School of Electrical and Electronic Engineering, Yonsei University Mar. 2018 - Aug. 2024

Dissertation: High-Performance Address Translation Mechanisms for

Graphics Processing Units (Advisor: Won Woo Ro)

Bachelor's Degree School of Electrical and Electronic Engineering, Yonsei University Mar. 2014 - Feb. 2018

PUBLICATIONS

Heliostat: Harnessing Ray Tracing Accelerators for Page Table Walks

Yuan Feng, Yuke Li, Jiwon Lee, Won Woo Ro, and Hyeran Jeon

(To appear) IEEE/ACM International Symposium on Computer Architecture (ISCA), 2025.

COSMOS: An LLC Contention Slowdown Model for Heterogeneous Multi-core Systems

Yongju Lee, Jaewon Kwon, Cheolhwan Kim, Enhyuk Jang, <u>Jiwon Lee</u>, Hyunwuk Lee, and Won Woo Ro (To appear) IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2025.

HashScape: Leveraging Virtual Address Dynamics for Efficient Hashed Page Tables

Won Hur, Jiwon Lee, Jaewon Kwon, Minjae Kim, and Won Woo Ro

IEEE Transactions on Computers (TC), 2025.

Marching Page Walks: Batching and Concurrent Page Table Walks for Enhancing GPU Throughput

Jiwon Lee*, Gun Ko, Myung Kuk Yoon, Ipoom Jeong, Yunho Oh, and Won Woo Ro

IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2025.

REC: Enhancing Fine-Grained Cache Coherence Protocol in Multi-GPU Systems

Gun Ko, <u>Jiwon Lee</u>, Hongju Kal, Hyunwuk Lee, and Won Woo Ro

Journal of Systems Architecture (JSA), Vol. 160, 103339, Mar. 2025.

Geneva: A Dynamic Confluence of Speculative Execution and In-Order Commitment Windows

Yanghee Lee, Jiwon Lee, Jaewon Kwon, Yongju Lee, and Won Woo Ro

IEEE/ACM Design Automation Conference (DAC), 2024.

SnakeByte: A TLB Design with Adaptive and Recursive Page Merging in GPUs

Jiwon Lee*, Ju Min Lee, Yunho Oh, William J. Song, and Won Woo Ro

IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2023.

Early-Adaptor: An Adaptive Framework for Proactive UVM Memory Management

Seokjin Go, Hyunwuk Lee, Junsung Kim, Jiwon Lee, Myung Kuk Yoon, and Won Woo Ro

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2023.

Analysis on Memory Access Patterns of Server-Class Workloads in Page- and Cache Line- Granularity

Kyeonghoon Lim, Minjae Kim, Jiwon Lee, and Won Woo Ro

International Conference on Electronics, Information, and Communication (ICEIC), 2023.

Performance Analysis of Criticality-Aware Out-of-Order Cores for Exploiting MLP

Yanghee Lee, **Jiwon Lee**, and Won Woo Ro

International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), 2023.

Adaptive Data Prefetcher with Probability Learning in LLC

Jusin Kim, Jiwon Lee, and Won Woo Ro

International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), 2023.

Reconstructing Out-of-Order Issue Queue

Ipoom Jeong, Jiwon Lee, Myung Kuk Yoon, and Won Woo Ro

IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022.

Analysis of DRAM-based Network of DRAM Swap Space Adopting Latency Hiding Technique

Hyoseong Choi, **Jiwon Lee**, Jeonghoon Choi, and Won Woo Ro

International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), 2022.

PIMCaffe: Functional Evaluation of a Machine Learning Framework for In-Memory Neural Processing Unit

Won Jeon, **Jiwon Lee**, Dongseok Kang, Hongju Kal, and Won Woo Ro

IEEE Access, Vol. 9, pp. 96629-96640, Jul. 2021.

Chapter Six - Deep learning with GPUs

Won Jeon, Gun Ko, <u>Jiwon Lee</u>, Hyunwuk Lee, Dongho Ha, and Won Woo Ro

Advances in Computers, Vol. 122, pp. 167-215, 2021.

PATENTS

Computing device and method of operating the same

Won Woo Ro, Minjae Kim, Kyeonghoon Lim, and Jiwon Lee

KR 10-2023-0193178

Memory management apparatus and method for UVM

Won Woo Ro, Seokjin Go, Junsung Kim, Hyunwuk Lee, and <u>Jiwon Lee</u>

KR 10-2023-0076606

Memory management unit and method of walking page table

Won Woo Ro, Jiwon Lee, Ipoom Jeong, Hongju Kal, Gun Ko, and Hyunwuk Lee

KR 10-2022-0175909, US 18/502,058, CN 202311700848.0

Swap memory device providing data and data block, method of operating the same, and method of operating electronic device including the same

Won Woo Ro, Hyoseong Choi, **Jiwon Lee**, and Jeonghoon Choi

KR 10-2022-0145399, US 18/350,148, CN 202311408257.6

Neural network processing method

Won Woo Ro, Hongju Kal, Cheonjun Park, Hyunwuk Lee, Ipoom Jeong, and <u>Jiwon Lee</u>

KR 10-2022-0041848

Controller, computing system including the same, and method of creating and searching page table entry for the same

Seongil O, Won Woo Ro, William Jinho Song, and Jiwon Lee

KR 10-2021-0054195, US 17/526,391, CN 202210082121.X

ON-GOING RESEARCH – PROJECT NAMES ONLY

Memory Management of Large-Scale Memory Space (Under Review) Efficient Address Translation Methods for GPUs (Under Review)

Accelerating Sparse Matrix Computations

Exploring Use Cases of CXL Memory Devices

Application of IOMMU Specifications

Identifying Bottlenecks in Serverless Environments

Analysis on Different Sparse Matrix Formats

Improving Unified Virtual Memory in GPUs

PROJECTS

Development of High Performance Multi-GPU Memory System

Mar. 2021 - Feb. 2024

Research project at Yonsei University joint with National Research Foundation of Korea

Development and Application of DRAM-based Memory Hierarchies

Sept. 2020 - Aug. 2023

Research project at Yonsei University joint with Samsung Electronics

Programmable Neural Network Processors

June 2018 - May 2022

Research project at Yonsei University joint with Samsung Research Funding and Incubation Center for Future Technology

PIM Core Technology and System Development for Data-intensive Applications

Mar. 2018 - Mar. 2020

Research project at Yonsei University joint with Samsung Electronics

Development of Reconfigurable Artificial Neural Network Accelerator and Instruction Set Architecture

Mar. 2018 - Feb. 2019

Research project at Yonsei University joint with Korea Electronics Technology Institute

ACADEMIC ACTIVITIES

External Review Committee

ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Summer Cycle 2026

Reviewer

ACM Transactions on Architecture and Code Optimization (TACO), 2025

Mentorship

Embedded Systems and Computer Architecture Lab, Yonsei University Industry-Academic Mentoring Program, Nov. 2024 - Present Intelligence System and Parallel Computer Architecture Lab Ewha Womans University Industry-Academic Mentoring Program, Jan. 2025 - Present

Teaching Assistant

EEE6611, System Design and Applications Lab, Yonsei University, Fall 2019

EEE4473, Embedded System Lab, Yonsei University, Spring 2019

EEE3535, Operating Systems, Yonsei University, Fall 2018

SCHOLARSHIPS AND AWARDS

Memory Division Graduate Fellowship

Sept. 2023 - Aug. 2024

Samsung Electronics

Excellent Graduate Researcher Scholarship

Feb. 2023

Yonsei University

National Scholarship for Science and Engineering

Korea Student Aid Foundation (KOSAF)

Mar. 2014 - Feb. 2018

Academic Excellence Award

Spring 2014

Yonsei University

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